AMENDMENTS TO THE CLAIMS

Please cancel claims 4 and 16 (renumbered as 15 by the Examiner), amend claims 1, 13-15 (now 12-14) and 17 (now 16). No new matter is believed to be introduced by the aforementioned claim amendments. The following listing of claims will replace all prior versions and listings of claims in the application.

1. **(Currently amended)** An optoelectronic device, comprising:

an integrated circuit having an automatically selectable data rate and configured to generate a loss of lock signal when an input data stream has a data rate out of range of an operational data rate at which the optoelectronic device is set, the integrated circuit comprising:

a data stream input for receiving the input data stream; and

a data rate select input configured to enable selection and setting of the operational data rate of the integrated circuit; and

a controller coupled to the data rate select input and configured to:

enable automatic adjustment of the operational data rate of the integrated circuit in response to receipt of the loss of lock signal; and

cease to adjust the selectable data rate once all selectable data rates have been attempted, whether or not the loss of lock signal has ceased.

2. **(Original)** The optoelectronic device as recited in claim 1, wherein the integrated circuit comprises one of: a clock and data recover integrated circuit; a multiplexer/demultimplexer integrated circuit; and, a serializer/deserializer integrated circuit.

3. **(Original)** The optoelectronic device as recited in claim 1, wherein the integrated circuit includes a sub-circuit that provide clock and data recovery for a plurality of data rates, the controller being configured to adjust the selectable data rate to each of the plurality of data rates.

4. **(Canceled)**

5. **(Original)** The optoelectronic device as recited in claim 1, wherein the controller and the integrated circuit reside together on a single chip.

6. **(Original)** The optoelectronic device as recited in claim 1, wherein the optoelectronic device is compatible with an input data rate of about 10 gigabits per second.

7. **(Original)** The optoelectronic device as recited in claim 1, wherein the optoelectronic device is compatible with the Fibre Channel protocol.

8. **(Original)** The optoelectronic device as recited in claim 1, wherein the optoelectronic device is compatible with at least one of: 2 gigabits per second Fibre Channel systems; and, 4 gigabits per second Fibre Channel systems.

9. **(Original)** A signal modification integrated circuit suitable for use in connection with an optoelectronic device, the signal modification integrated circuit comprising:

a receive circuit configured to operate at any one of a plurality of automatically selectable data rates and further configured to generate a loss of lock signal when a data stream associated with the receive circuit has a data rate out of range of an operational data rate at which the optoelectronic device is set, and the transmit circuit being configured to set the operational data rate of the optoelectronic device to successive data rates included in the plurality of automatically selectable data rates until one of the following occurs: the loss of lock signal asserted by the receive circuit ceases; or, each data rate in the plurality of automatically selectable data rates has been set; and

a transmit circuit configured to operate at any one of a plurality of automatically selectable data rates and further configured to generate a loss of lock signal when a data stream associated with the transmit circuit has a data rate out of range of an operational data rate at which the optoelectronic device is set, and the transmit circuit being configured to set the operational data rate of the optoelectronic device to successive data rates included in the plurality of automatically selectable data rates until one of the following occurs: the loss of lock signal asserted by the transmit circuit ceases; or, each data rate in the plurality of automatically selectable data rates has been set.

10. **(Original)** The signal modification integrated circuit as recited in claim 9, wherein the signal modification integrated circuit comprises a clock data recover integrated circuit that includes an oscillator serving as a reference clock.

11. **(Original)** The signal modification integrated circuit as recited in claim 9, wherein the plurality of automatically selectable data rates includes the data rates: about 4 Gb/s; and, about 2 Gb/s.

[[13]] 12. **(Currently amended)** The signal modification integrated circuit as recited in claim 9, wherein the receive circuit comprises one of: a receive CDR; a demultiplexer; and, a serializer.

[[14]] 13. **(Currently amended)** The signal modification integrated circuit as recited in claim 9, wherein the transmit circuit comprises one of: a transmit CDR; a multiplexer; and, a deserializer.

[[15]] 14. **(Currently amended)** A method for automatically selecting and setting an operational data rate of an optoelectronic device, the method comprising:

receiving an input data stream having an input data rate;

generating a loss of lock signal if the input data rate does not fall within a predetermined deviation from an operational data rate of the optoelectronic device, the operational data rate comprising one data rate in a range of automatically selectable data rates associated with the optoelectronic device;

detecting the loss of lock signal, if generated, and resetting the automatically selectable data rate of the optoelectronic device to a new data rate; [[and]]

repeating the detection and resetting processes until: a data rate has been set that causes deassertion of the loss of lock signal; or, all data rates in the range of automatically selectable data rates have been set without causing deassertion of the loss of lock signal; and

setting a bypass if all automatically selectable data rates in the range have been set without causing deassertion of the loss of lock signal.

16. **(Canceled)**

[[17]] 16. **(Currently amended)** A CDR integrated circuit suitable for use in connection with an optoelectronic device, the CDR integrated circuit comprising:

a first circuitry portion configured to operate at any one of a plurality of automatically selectable data rates and further configured to generate a loss of lock signal when a data stream associated with the first circuitry portion has a data rate out of range of an operational data rate at which the optoelectronic device is set, and the first circuitry portion being configured to set the operational data rate of the optoelectronic device to successive data rates included in the plurality of automatically selectable data rates until one of the following occurs: the loss of lock signal asserted by the first circuitry portion ceases; or, each data rate in the plurality of automatically selectable data rates has been set; and

a second circuitry portion configured to operate at any one of a plurality of automatically selectable data rates and further configured to generate a loss of lock signal when a data stream associated with the second circuitry portion has a data rate out of range of an operational data rate at which the optoelectronic device is set, and the second circuitry portion being configured to set the operational data rate of the optoelectronic device to successive data rates included in the plurality of automatically selectable data rates until one of the following occurs: the loss of lock signal asserted by the second circuitry portion ceases; or, each data rate in the plurality of automatically selectable data rates has been set, the first circuitry portion and the second circuitry portion being implemented together as a single IC.